REMARKS

Reconsideration of the above-identified patent application is requested in view of the remarks that follow.

In the April 23, 2004, Office Action in this application, the Examiner objected to the drawings. Specifically, the Examiner states that Fig. 3 does not include the reference numbers identified in the specification.

Enclosed herewith, Applicant provides a copy of Fig. 3 marked in red ink to identify proposed changes that add reference numbers to Fig. 3, as suggested by the Examiner. Approval of the propose amendments is hereby requested.

The Examiner rejected claims 1-3 under 35 U.S.C. §102(e) as being anticipated by the Sang et al. '636 patent. For the reason set forth below, this rejection of original claims 1-3 is traversed.

Applicant's original independent claim 1 is directed to a switch router circuit that includes a multi-port store/switch memory array that is connected to receive packet payloads of incoming data packet. The multi-port store/switch memory array recited in claim 1 includes a plurality of storage areas, with each distinct storage area being associated with a corresponding media access control (MAC) unit such that the packet payload of an incoming data packet received by a specific MAC unit is stored in a corresponding specific storage area of the multi-port store/switch memory array.

Independent claim 1 further recites that the switch router circuit includes an arbitrator that is connected to the multi-port store/switch memory array. The recited arbitrator, in the event that the destination port identified by the packet header of an incoming data packet is included within the plurality of MAC units of the switch/router circuit, arbitrates direct connection of the specific memory array storage area associated with the specific MAC unit that receives the incoming data packet to the specific MAC unit identified as the destination port. As a result,

direct transfer of the packet payload of the incoming data packet to the destination port is facilitated.

The Examiner cites the Sang et al. reference as teaching these features of Applicant's claim 1 invention. Specifically, the Examiner refers to column 6, lines 54-67 of the Sang et al. reference for reference to packets received by the MAC modules being sent to a store area in the external memory 36 and for reference to each of the storage areas of the external memory being associated with each of the MAC modules using frame pointers, which link a MAC unit to the area in which a received packet has been stored in the external memory 36.

Column 6, lines 54-67 of the Sang et al. patent read as follows:

> "Each of the receive MAC modules 70_a, 70_b, 72_a, and 72_b include queuing logic 74 for transfer of received data from the corresponding internal receive FIFO to the external memory 36 and the rules checker 40. Each of the transmit MAC modules 70_c, 70_d, 72_c, and 72_d includes a dequeuing logic 76 for transferring data from the external memory 36 to the corresponding internal transmit FIFO, and a queuing logic 74 for fetching frame pointers from the free buffer queue 64. The queuing logic 74 uses the fetched frame pointers to store receive data to the external memory 36 via the external memory interface controller 44. The frame buffer pointer specifies the location in the external memory 36 where the received data frame will be stored by the receive FIFO."

Applicant submits that while this section of the Sang et al. reference discloses the use of a internal receive FIFO for buffering incoming data packets, and also discloses the use of a frame pointer to maintain the location in the external memory 36 in which a received data packet has been stored, nothing in this portion of the Sang et al. reference has either teaches or suggests the specific aspects of the multi-port store/switch memory array or the arbitrator elements recited in Applicant's claim 1. Specifically, nothing in the cited section of the Sang et al. reference either teaches or suggests a multi-port store/switch memory array that includes a plurality of distinct storage areas wherein in each specific storage area is associated with a corresponding specific MAC unit. Further, nothing in the Sang et al. reference either teaches or suggests an arbitrator that arbitrates direct connection of the specific memory array storage area associate with MAC unit that receives the incoming data packet to the specific MAC unit identified as destination port by the packet header of the data packet.

The Examiner refers to column 4, lines 33-46 and to column 5, line 53 to column 6, line 12 of the Sang et al. reference as disclosing Applicant's arbitrator connected to a multi-port

store/switch memory array and including characteristic which allow it to arbitrate direct connection of the memory arrays storage area associated with the MAC unit that receives the incoming data packet to the MAC unit identified as the destination port.

Column 4, line 33-46 of the Sang et al. reads as follows:

> "Fig. 2 is a block diagram of the multiport switch 12. The multiport switch 12 contains a decision making engine 40 that performs frame forwarding decisions, a switching subsystem 42 for transferring frame data according to the frame forwarding decisions, an external memory interface 44, management information base (MIB) counters 48_a and 48_b (collectively 48), and MAC (media access control) protocol interfaces 20 and 24 to support the routing of data packets between the Ethernet (IEEE 802.3) ports serving the network stations 14 and the gigabit node 22. The MIB counters 48 provide statistical network information in the form of management information base (MIB) objects, to an external management entity controlled by a host CPU 32, described below."

Column 5, line 53 to column 6, line 12 of the Sang et al. reference reads as follows:

> "The internal rules checker 40 outputs a forwarding decision to the switch subsystem 42 in the form of a forwarding descriptor. The forwarding descriptor includes a priority class identifying whether the frame is high priority or low priority, a port vector identifying each MAC port that should transmit the data frame, receive port number, an untagged set, VLAN information, vector identifying each MAC port that should include VLAN information during transmission, opcode, and frame pointer. The format of the forwarding descriptor will be discussed further with respect to Fig. 7. The port vector identifies the MAC ports to receive the data frame for transmission (e.g., 10/100 MAC ports 1-12, Gigabit MAC port, and/or Expansion port). The port vector FIFO 56 decodes the forwarding descriptor including the port vector, and supplies the frame pointer to the appropriate output queues 58 that correspond to the output MAC ports to receive the data frame transmission. In other words, the port vector FIFO 56 supplies the frame pointer on a per-port basis. The output queues 58 give the frame pointer to a dequeuing block 76 (shown in Fig. 3) which fetches the data frame identified in the port vector from the external memory 36 via the external memory interface 44, and supply the retrieved data frame to the appropriate transmit FIFO of the identified ports. If a data frame is to be supplied to a management agent, the frame pointer is also supplied to a management queue 68, which can be processed by the host CPU 32 via the CUP interface 50."

Again, Applicant submits that nothing in the cited section of the Sang et al. reference teach an arbitrator that is connected to a multiport store/switch memory array and includes structural functionality for arbitrating direct connection for the specific memory arrays storage

area associated with the MAC unit that receives an incoming data packet to the specific MAC unit identified as the destination port.

For the reason set forth above, Applicant submits that original independent claim 1 is novel in view of, and therefore not anticipated by, the Sang et al. disclosure.

The Examiner has rejected Applicant's original claim 4 under 35 U.S.C. 103(a) as being unpatentable over the Sang et al. in view of the Poteet et al. '240 patent and in further view of the Bansal et al. '637 patent. The Examiner relies on the Sang et al. reference as teaching the major features of the claim 4 invention, but states Sang et al. do not disclose that the multi-port store/switch memory array recited in Applicant's claim 4 facilitates double-ended write of incoming packets. The Examiner relies on the Poteet et al. reference as disclosing the use of double-ended write in a memory system. The Bansal et al. reference is rely upon as disclosing the use of buffered multi-port read of outgoing packet payloads.

Applicant's original claim 4 that depends from independent claim 1. For the reason set forth above with respect to independent claim 1, Applicant submits that the Sang et al./Poteet et al./Bansal et al. reference combination neither teaches nor suggests either a multi-port store/switch memory array or an arbitrator element as recited in Applicant's original claim 4.

Claim 5 has been rejected under 35 U.S.C. 103(a) as being over Sang et al. in view of the Majos et al. '366 patent. Majos is cited in combination with the Sang et al. reference as disclosing a memory using double port write and double port read.

Applicant's original claim 5 depends from independent 1. Therefore, for reasons set forth above with respect to independent claim 1, Applicant submits that the original claim 5 recites subject matter that patentably distinguishes over the Sang et al./Majos et al. reference combination.

For the reasons set forth above, Applicant is of the good faith belief that all claims now present in this application patentably distinguish over the prior art. Therefore, it is requested that this application be passed to allowance.

Respectfully submitted,

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Dated: September 30, 2004

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